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ABSTRACT OF THE DISCLOSURE

The present invention concerns an apparatus comprising a memory, a logic circuit and a multiplexer. The memory generally comprises a first address space configured as read only and a second address space configured as read and write. The memory  
5 returns a first data item in response to a first address within the first address space. The logic circuit may be configured to (i) deassert a command signal in response to the first address not matching any of a plurality of predetermined addresses and (ii) generate a first branch instruction and assert the command signal  
10 in response to the first address matching one of the predetermined addresses in response to the matching. The multiplexer may be configured to select the first data item from the memory or the first branch instruction from the logic circuit in response to the command signal.